(51) International Patent Classification ^{6} : H04J 3/16, 3/22	**A1**	(11) International Publication Number: **WO 99/59279** (43) International Publication Date: 18 November 1999 (18.11.99)

(21) International Application Number: PCT/US99/10366

(22) International Filing Date: 11 May 1999 (11.05.99)

(30) Priority Data:
09/075,669   11 May 1998 (11.05.98)   US

(63) Related by Continuation (CON) or Continuation-in-Part
(CIP) to Earlier Application
US   09/075,669 (CON)
Filed on   11 May 1998 (11.05.98)

(71) Applicant *(for all designated States except US)*: ESS TECH-
NOLOGY, INC. [US/US]; Barton Oaks Plaza Four, Suite
290, 901 South Mopac, Austin, TX 79746 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: SARTAIN, Daryl
[US/US]; 6406 Copperlily CV, Austin, TX 78759 (US).
SCULLEY, Terry [US/US]; 5009 Trading Bend Drive,
Austin, TX 78735 (US).

(74) Agent: HARRIS, Scott, C.; Fish & Richardson P.C., Suite
1400, 4225 Executive Square, La Jolla, CA 92037 (US).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG,
BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB,
GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG,
KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK,
MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA,
ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ,
UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD,
RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK,
ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI
patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR,
NE, SN, TD, TG).

Published
With international search report.

(54) Title: VARIABLE CODEC FRAME LENGTH

(57) Abstract

The invention manages an input buffer (111) of a coder System (110), as shown in the Figure. The contents of the buffer (111) is
monitored in a monitor (133), generating an underflow signal when the buffer is empty or has an amount below a threshold and an overflow
signal when the buffer is full or above a threshold. As a result of this other parts of the codec (110) are controlled to accommodate differing
data rates. This includes lengthing or shortening the sample frames received from the input buffer (111) by using a variable interpolation
filter (145) and a controller (137), increasing or decreasing the sample rate per frame. Instead of variable interpolation filter (145) the
interpolation filter may generate a fixed number of oversamples per input sample. In both ways, distortion due to differences in data rates
is reduced.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav	TM	Turkmenistan
BF	Burkina Faso	GR	Greece		Republic of Macedonia	TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's	NZ	New Zealand		
CM	Cameroon		Republic of Korea	PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

- 1 -

VARIABLE CODEC FRAME LENGTH

TECHNICAL FIELD

This invention relates to compensating data rates,
5   and more particularly to modifying asynchronous data
rates to compensate for data rate differences in
successive blocks of a circuit.

BACKGROUND

Data sent to a codec may be sourced at an
10 asynchronous rate. Overflow or underflow of the data may
result if the data rate in one portion of a circuit is
different from the data rate in a following section.

For example, audio data sent via a streaming pipe
over the internet may be played as it is downloaded,
15 e.g., using the MP3 standard. Downloading starts, a
buffer is accumulated, and then the data is decompressed
and played while the remainder downloads. The rate at
which the data may be received from the internet server
is directly dependent on the type of modem connection and
20 how variable that connection is over time. As time goes
on, a poor connection may lead to, for example, loss of
data packets. As packets are retransmitted, the host
side buffer may be drained and the data may run out.

This possible problem is described in the context
25 of a digital-to-analog converter ("DAC") system 10. A
DAC system 10 includes a digital portion 19 and an analog
portion 21. If the DAC is an oversampling delta-sigma
type, the digital portion will typically include an
interpolator 13. The interpolator 13 includes an
30 interpolation filter 23 and a sample-and-hold circuit 25.

- 2 -

The interpolation filter 23 increases the sample
rate and removes or significantly attenuates energy at
$f_s/2$ and above, where f_s is the input sampling frequency.
The output of the interpolation filter 23 is processed
5   through the sample-and-hold circuit 25 to provide an
over-sampled output.

The output of the sample-and-hold circuit 25 is
sent to modulator 15 which converts the oversampled
signal into a one-bit data stream. The modulator 15 may
10   be a delta-sigma modulator which provides good low level
performance and can act as a one-bit digital quantizer.

The one-bit data stream is sent to a one-bit DAC
29. The signal from the one-bit DAC 29 is then fed to
the analog portion 21.

15   The analog portion 21 includes at least a filter
17. The filter 17 may be an analog low pass filter such
as a switched capacitor filter.

A typical rate at which data may stream through
the DAC system 10 may be 48 kHz. If this data is then
20   passed to a downstream circuit which operates at a
different speed, such as a constrained pipe, the data
will either back up (if the downstream circuit operates
at a lower speed), or stall (if the downstream circuit
operates at a higher speed). For example, data may be
25   recorded at 48 kHz and subsequently stored. The data may
then be streamed to a system through a constrained pipe
at an average rate of 46 kHz. The output will
periodically stall because the data rate through the
constrained pipe cannot be increased.

30   The present invention addresses the above problems
by dynamically compensating for differences in data
rates. In one embodiment, the status of an input buffer
is monitored and used to change the number of oversamples

- 3 -

within a frame. In another embodiment, the input buffer is still monitored but a high frequency clock in the system is used to stall the codec for one clock. In both embodiments, distortion due to differences in data rates

5 is reduced.

In one embodiment, the method includes steps of receiving samples of a signal at a sampling rate, oversampling the sampled signal to generate a prespecified number of oversamples per a frame, and

10 deleting or repeating one or more of the oversamples per frame to remove the overflow or underflow condition.

In another embodiment, the method includes steps of receiving samples of a signal at a sampling rate and oversampling the sampled signal to generate one of a

15 prespecified number of oversamples per a frame. The prespecified number is equal to a nominal number in the absence of an overflow or underflow condition, the prespecified number is greater than the nominal number in an underflow condition, and the prespecified number is

20 less than the nominal number in an overflow condition.

In another embodiment, the method includes steps of receiving samples of a signal at a sampling rate, oversampling the sampled signal to generate a prespecified number of oversamples per a frame; and

25 stalling the circuit for a number of cycles of the master clock to remove the overflow or underflow condition.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and

30 advantages of the invention will be apparent from the description and drawings, and from the claims.

- 4 -

DESCRIPTION OF DRAWINGS

FIG. 1 is a schematic block diagram of a prior art DAC system.

FIG. 2 is a schematic block diagram of a DAC
5 system according to an embodiment of the present invention showing control of an input buffer.

FIG. 3 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of an input buffer via a
10 variable interpolation filter.

FIG. 4 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of an input buffer via an interpolation filter and a frame controller.

15   FIG. 5 is a schematic block diagram of a DAC system according to an embodiment of the present invention showing control of a stall condition by using a master clock to stall the codec for a clock cycle.

FIG. 6 is a flowchart for an adaptive control loop
20 according to an embodiment of the present invention.

FIG. 7 shows a flowchart for the detection of an appropriate peak frame for use in inserting or removing oversamples at random rates.

Like reference numbers and designations in the
25 various drawings indicate like elements.

- 5 -

DETAILED DESCRIPTION

The present invention solves many of the aforementioned problems by, in part, managing an input buffer to the codec. Fig. 2 shows such an input buffer

5   in the context of a DAC system 110. In this DAC system 110, digital data flows to input buffer 111 which in turn directs the data to digital portion 119. The digital portion 119 includes an interpolator 113 having an interpolation filter 123 and a sample-and-hold circuit

10 125. The data flows to a modulator 115 and a one-bit DAC 129. At this point the analog data is coupled to the analog portion 121 which includes a filter 117. The analog data then may flow out of the DAC system 110 and into downstream circuitry 131.

15   The contents of the input buffer 111 may be tested in a monitor 133. The monitor may, for example, generate an underflow signal when the input buffer is empty or has an amount of data below some low threshold. It may also generate an overflow signal when the input buffer is full

20 or has an amount of data above some high threshold. The results of the testing may be used to control various parts of the DAC system 110, or various parts of a circuit in which the DAC system 110 is located, in accordance with the principles of the invention as

25 exemplified below. In particular, the status of the contents of the input buffer 111 as tested by monitor 133 can be used to make adjustments to other parts of the system in order to accommodate differing data rates. The way in which such adjustments are made are presented

30 below as example embodiments of the invention.

The status of the input buffer 11 can indicate whether the downstream rate is greater than or less than the upstream rate. For example, if the input buffer 111

is full or nearly full, the downstream rate is likely to be less than the upstream rate. In other words, the data rate is too high to be accommodated by all downstream circuitry beginning at the digital portion 119. If the

5 input buffer 111 is empty or nearly so, the downstream rate is likely greater than the upstream rate. In general, it is preferable to allow the input buffer 111 to operate without running empty.

Management of the input buffer 111 may include

10 lengthening or shortening the sample frames to accommodate the different data rates. In a first embodiment, the codec frame length is varied. In this embodiment and others, the invention will be described in the context of a DAC system. However, one skilled in the

15 art will recognize other systems in which the invention may be employed. For example, the invention may be employed in the context of an ADC or other devices in which both push-data and pull-data are present, such as a television tuner card in a computer. Of course, even the

20 tolerance of a standard crystal oscillator in a system leads to differences in data rates.

The following definitions are used herein. When information is available to a system for immediate access on-demand, it is categorized as "pull data". This on-

25 demand data may be from any type of storage medium that provides a feedback path for control. Examples of this type include HDD, CD, DVD, PC memory systems, and many others.

When information is transferred or broadcast

30 without regard to its reception and no data flow control feedback, it is categorized as "push data". This data type will not slow, stop, or retransmit for the receiver; therefore, the receiver must keep pace. Examples of this

- 7 -

type include television broadcast, radio broadcast, and
internet multicast.

It is also noted that while 128 oversamples is
used throughout this description, the actual number may
5   vary with the application. A system with any number of
oversamples may effectively use the method of the
invention.

One way of constructing this embodiment is shown
by a DAC 210 in Fig. 3. This embodiment involves the use
10 of a variable interpolation filter 145. As noted above,
the interpolation filter is in part responsible for
increasing or decreasing the sample rate. The variable
interpolation filter 145 can generate extra or fewer
oversamples for the given frame. In most cases, one
15 extra or one fewer would be appropriate. By performing
this in accordance with the oversampling rate, the
distortion is reduced.

The digital portion 119 affects the input buffer
111 by way of data overflowing in the input buffer 111 or
20 by the input buffer 111 running empty. In other words,
the digital portion affects the input buffer 111 by
overflowing or stalling. In a different embodiment, the
digital portion 119 may actually provide a signal to
input buffer 111 or to a monitor 133 within the input
25 buffer 111. This signal would then provide an indication
of the state of the data rate in the downstream circuitry
131 or even downstream of the downstream circuitry 131.
Preferably, the input buffer never completely overflows
or stalls. The monitor detects when these conditions are
30 close to occurring and signals the digital portion 119 to
alter its number of oversamples per frame. The monitor,
in this fashion, provides signals identifying a "near
overflow" or a "near stall" condition.

- 8 -

Once a signal is received indicating that a near
stall or overflow condition has occurred, the signal is
sent to a controller 137 within the variable
interpolation filter 145. This signal may be sent from
5 the monitor 133 within buffer 111. Once received, the
signal causes the variable interpolation filter 145 to
alter the number of oversamples per frame. In other
words, rather than having the interpolation filter
provide a uniform number of additional oversamples per
10 input sample, the variable interpolation filter 145
inserts or deletes oversamples as required to avoid the
stall or overflow condition described above. For
example, if variable interpolation filter 145 usually
insert 128 oversamples per each input sample, a near
15 overflow condition may cause the variable interpolation
filter to insert only 127. Conversely, if variable
interpolation filter 145 usually inserts 128 oversamples
per each input sample, a near stall condition may cause
the variable interpolation filter to insert 129. An
20 appropriate number of coefficients is chosen for the
extra or fewer oversamples. Appropriate control over the
number of oversamples created is provided by the
controller 137. In other words, in the example above,
instead of 128 coefficients being chosen, 127 or 129
25 coefficients would be chosen.

In a different embodiment, rather than having a
variable interpolation filter generate more or less
oversamples per input sample, the interpolation filter
may generate a fixed number of oversamples per input
30 sample. However, once oversampling is completed, a
particular oversample may be deleted or repeated in order
to switch to a 127/129 oversample frame if required by a
near overflow or near stall condition. This embodiment

- 9 -

is shown in Fig. 4. In this figure, a DAC 310 has an
interpolation filter 143 with two stages: an oversampling
portion 139 and a frame controller 141. The oversampling
portion 139 provides the requisite number of oversamples

5   per sample, e.g., 128. The frame controller 141 deletes
or repeats an oversample according to the stall or
overflow condition. The determination of when the frame
controller 141 is required to edit the number of
oversamples may be made by the input buffer monitor 133

10 or by some other source, and is carried out via a
controller 147. Of course, the controller 147 and the
frame controller 141 may be within the same or different
blocks of the circuit.

The location within the frame of the oversample
15 that is deleted or inserted may be chosen in a random
manner to avoid the generation of unwanted tonal
components. Such a method is described below. If tonal
component generation is not a factor, the location of the
oversample chosen may be arbitrary. For example, the

20 first oversample or the last oversample may always be the
oversample chosen.

In both of these embodiments, any error introduced
by the removal or addition of oversamples is spread over
all (approximately) 128 oversamples. In other words,

25 errors occur to oversampled values rather than to raw
input samples so as to preserve data integrity.
In yet another embodiment, as shown by Fig. 5, no extra
or fewer oversamples are created, nor are a set number of
oversamples subject to a repetition or deletion of any

30 one oversample. In this embodiment, the codec is stalled
for one or more clock cycles. This embodiment is
applicable to those situations where the interpolation
filter creates an additional oversample, rather than

- 10 -

where the interpolation filter causes the deletion of an
oversample or the creation of fewer than the nominal
number of oversamples.

Fig. 5 shows a master clock 151 controlling the
5 interpolation filter 149. The master clock 151 may, of
course, also control various other aspects of the system.
Moreover, the master clock 151 may be used to create
other clocks whose rates are either the same or are based
on the master clock 151. The presence and rates of these
10 other clocks depend on the requirements of the system.

In this embodiment, the clock with the highest
rate, here denoted MILK 151, may be used as the basis for
the stall procedure.

The MILK 151 may be caused to stall for one or
15 more clock cycles or alternatively for one or more phases
of the MILK 151. In this way, the downstream circuitry
131 may be allowed time to process the overflow
oversamples and thus remove the overflow condition. The
resulting frames in the codec would be slipped.
20 This embodiment may produce less distortion than the
sampling based embodiments above. For example, a typical
master clock rate may be MILK = 24.576 MHZ. Using a
half-clock stall leads to:

$$\frac{(2)(24.576 \; MHz)}{48 \; kHz} = 1024 \; \rightarrow \; 20 \; \log \; 1024 \; = 60 \; dB$$

In this example, the clock stall thus provides 60
25 DB less distortion than the sample-based solutions
because the master clock has a much higher resolution
than the sample rate. It should be noted in this
embodiment that the bus interface would need to operate

- 11 -

asynchronously such that the bus would not see the stall
of the MILK 151.

     In these embodiments, the monitor 133 of input
buffer 111 may be used to detect and correct overflows or
5 underflows in several ways. For example, low and high
thresholds may be set and used to trigger the change in
the frame length as described above. The resulting
change in data consumption rate causes the input buffer
111 to move back between the low and high thresholds and
10 the oversamples per frame are reset to nominal. If the
tested parameter is not reset (due, e.g., to a large
mismatch in data rates) the frame length may be adjusted
further to increase the rate of recovery.

     In another modification, rather than have a preset
15 number of oversamples per frame, monitor 133 may consider
the number of oversamples per frame to be a variable
which is usually at a steady-state value but which varies
with overflows and underflows. In this method, termed
herein the "loop offset mode", thresholds are still set
20 at low and high points but the number of oversamples per
frame no longer tends towards a fixed value. Rather, the
number of oversamples per frame tends towards whatever
value is required to reduce the overflow or underflow.
For example, if the tested parameter indicates an
25 underflow (the low threshold is passed), the number of
oversamples per frame may increase to 129 from 128. This
causes the underflow to be eliminated. Rather than move
back to 128, the number of oversamples per frame stays at
129 until the buffer falls below the low threshold again
30 or above the high threshold. The loop offset mode may be
especially useful when the sourcing rate is significantly
different from the playback rate.

- 12 -

The error difference provided by adjusting the
samples at 128x oversampling are two orders of magnitude
greater than error concealment performed at the sample
rate, reducing distortion effects by over 40 DB (e.g., 20

5   log 128 = 48 DB). Of course, the codec internal frame
should be fully independent of the audio input frame.

Fig. 6 shows a flowchart for an adaptive control
loop used in the codec input buffer, and in particular an
operation of an adaptive error concealment codec.

10 Thresholds are established for both overflow and
underflow conditions. The first step is subsystem
initialization 201. A decision 203 is then made as to
whether the adaptive circuit is enabled. This decision
ensures that the codec has a mode that is compatible with

15 industry codecs. If the adaptive circuit is enabled,
then a determination is made as to whether the "loop
offset mode" is enabled (step 205). As mentioned above,
the loop offset mode is particularly suitable when rates
vary significantly in different portions of a system

20 because the frame size may continue to be modified in a
rate-adaptive manner. If the loop offset mode is
enabled, then the determination of overflow (step 207) or
underflow occurs (step 209). For example, if the input
buffer falls below the low threshold (underflow step

25 209), each consecutive frame in which the buffer is below
the low threshold has a frame length that is increased
(step 211), e.g., by one oversample value. Once the
playback rate matches the source rate, the buffer status
moves back above the low threshold and stabilizes at a

30 frame size appropriate for the incoming data. If an
overflow condition occurred, each consecutive frame in
which the buffer is above the high threshold has a frame
length that is decreased (step 213), e.g., by one

- 13 -

oversample value. In both the case of an underflow and
where the number of oversamples per frame is decreased, a
test for an empty buffer (step 215) may occur. In both
underflows and overflows, the frame size is adjusted to
5   compensate and the final size of the frame is calculated
(step 219) from the loop responses. The net effect is
that the data is played at a rate that is different from
its recorded rate; however, empty frames do not occur,
nor do overflows.

10   If the loop offset mode is not enabled, then the
frame length is reset, for each frame, to the preset
value (e.g., 128 oversamples per frame) (step 217). For
small drifts between the source data and the playback,
this way may be preferred and allows for instantaneous
15 correction with low distortion. It should be noted that
this flowchart is only representative of one of the
several methods available.

It should also be noted that when oversample
insertion or removal occurs at a periodic rate, there is
20 a tonal component generated at the rate of insertion or
removal. If the rate of insertion or removal is
randomized, the tonal energy will be distributed over a
wide range and the overall tonal component will be small
enough to be unnoticeable.

25   In order to achieve a random insertion or removal
rate, the timing in which the interpolator may be caused
to insert or remove an oversample may be adjusted. In
particular, when the interpolator receives a request for
an oversample skip or repeat, the interpolator may simply
30 insert or remove the oversample accordingly; however,
this may lead to the tonal generation above. Instead,
the interpolator may choose to wait to insert or remove
the oversample until a prespecified time. The

- 14 -

appropriate prespecified time to insert or remove an
oversample may be when the frame's oversamples have an
extreme value (i.e., an approximately zero slope). At
these points, addition or removal of oversamples does not
5 result in a significant change in the frequency
components. A certain time period is added but little
distortion is added.

One method of determining the extreme value is
shown in Fig. 7. Fig. 7 shows an extremal detection
10 flowchart. Initially, an extremal flag is reset (step
301). The first test may be for a negative slope of the
current frame (step 303). If the slope is negative, then
the following frame slope is tested (step 305). If this
slope is not negative, then the extremal flag is set
15 (step 307) and the insertion or removal may proceed. If
this slope is negative, other sample processing may occur
(step 309) and the slope detect procedure is begun again.

If the current frame slope is not negative, then
the following frame slope is tested (step 311). If this
20 slope is negative then the extremal flag is set (step
313) and the insertion or removal may proceed. If this
slope is not negative, other sample processing may occur
(step 309) and the slope detect procedure is begun again.

Again it is noted that this flowchart is only
25 representative of one of the several methods available.
It should be noted that if no extremal is available after
waiting a prespecified period of time, the interpolator
may be forced to insert or remove the oversample despite
the lack of an extremal frame (e.g., a 20 Hz input with
30 extremes every 25 ms).

It is noted that the source data frame sync and
the internal codec frame sync do not need to sync-up
because the incoming stream is destined for the analog

- 15 -

domain.   Thus, in the context of the system which
generated the incoming stream, there is no longer a frame
of discrete reference.   The data is in continuous time,
allowing full decoupling of the data bus frame sync from
5 the internal codec frame sync.

Example of Error Accumulation

The accumulated error, when an extra audio
oversample is created (to account for data rate
disparities in a system), may be estimated as follows.
10 The master clock for audio may be operated at, e.g., 48
kHz x 128 x 2 = 12.288 MHZ.   The oversampling rate is 48
kHz times the number of oversamples per frame (128) =
6.144 MHZ.   With the oversample rate of 128, if the frame
were lengthened to 129, the number of audio samples per
15 second would be

$$\frac{12.288 \; MHz}{2 \times 129} = 47,628$$

For typical oscillators, at a 50 PPM / clock
accuracy, a 100 PPM error could result from the two
clocks.   At 48 kHz, this results in 4.8 samples per
second drift between subsystems.   At 1/10,000 of the
20 distribution of 128 oversamples, this leads to 10,000/128
or 78.   In other words, one extra or fewer oversamples
would be generated each 78 audio samples.

A number of embodiments of the present invention
have been described.   Nevertheless, it will be understood
25 that various modifications may be made without departing
from the spirit and scope of the invention.   For example,
the invention may be utilized in a number of other
devices besides DACs.   Moreover, the invention is

- 16 -

intended to encompass any sample rates, oversample rates, master clock rates, DAC bit resolution, etc. The values used here are only for illustrative purposes and should not be considered limiting. Accordingly, other
5 embodiments are within the scope of the following claims.

- 17 -

WHAT IS CLAIMED IS:

1.   A method of dynamically compensating for an overflow
condition in a circuit, comprising:
        sampling a signal at a sampling rate;
5   oversampling the sampled signal to generate a
prespecified number of oversamples per a frame;
        changing an amount of oversampling per frame to
at least partially compensate for the overflow
condition.

10 2.   The method of claim 1, further comprising the step
of detecting the overflow condition by testing the
status of an input data buffer.

3.   The method of claim 1, further comprising the step
of detecting the overflow condition by testing the
15   status of a data buffer in a portion of a downstream
circuit.

4.   The method of claim 1, further comprising the step
of generating a number of coefficients equal to the
prespecified number.

- 18 -

5. An apparatus for dynamically compensating for an overflow condition in a circuit, comprising:

an interpolation filter to generate a fixed number of oversamples for an input sample;

a frame controller coupled to the interpolation filter to delete at least one of the number of oversamples generated;

a buffer for holding the input sample prior to the generation of oversamples; and

a monitor to test the buffer, the monitor coupled to the frame controller to provide the frame controller with an overflow condition in a circuit.

6. A method of dynamically compensating for an overflow condition in a circuit, comprising:

sampling a signal at a sampling rate;

oversampling the sampled signal to generate one of a prespecified number of oversamples per a frame, the prespecified number equal to a nominal number in the absence of an overflow condition, the prespecified number less than the nominal number.

7. The method of claim 6, wherein the prespecified number is equal to the nominal number minus one oversample.

8. The method of claim 6, further comprising the step of detecting the overflow condition by testing the status of an input data buffer.

- 19 -

9. The method of claim 6, further comprising the step of detecting the overflow condition by testing the status of a data buffer in a portion of a downstream circuit.

5   10. The method of claim 6, further comprising the step of generating a number of coefficients equal to the prespecified number.

11. An apparatus for dynamically compensating for an overflow condition in a circuit, comprising:

10   a variable interpolation filter to generate oversamples for an input sample;

      a controller coupled to the variable interpolation filter to control the number of oversamples generated;

15   a buffer for holding the input sample prior to the generation of oversamples; and

      a monitor to test the buffer, the monitor coupled to the controller to provide the controller with an overflow condition in a circuit.

20   12. A method of dynamically compensating for an underflow condition in a circuit having a master clock, comprising:

      sampling a signal at a sampling rte;

      oversampling the sampled signal to generate a

25   prespecified number of oversamples per frame; and

      stalling the circuit for a number of cycles of the master clock to remove the underflow condition.
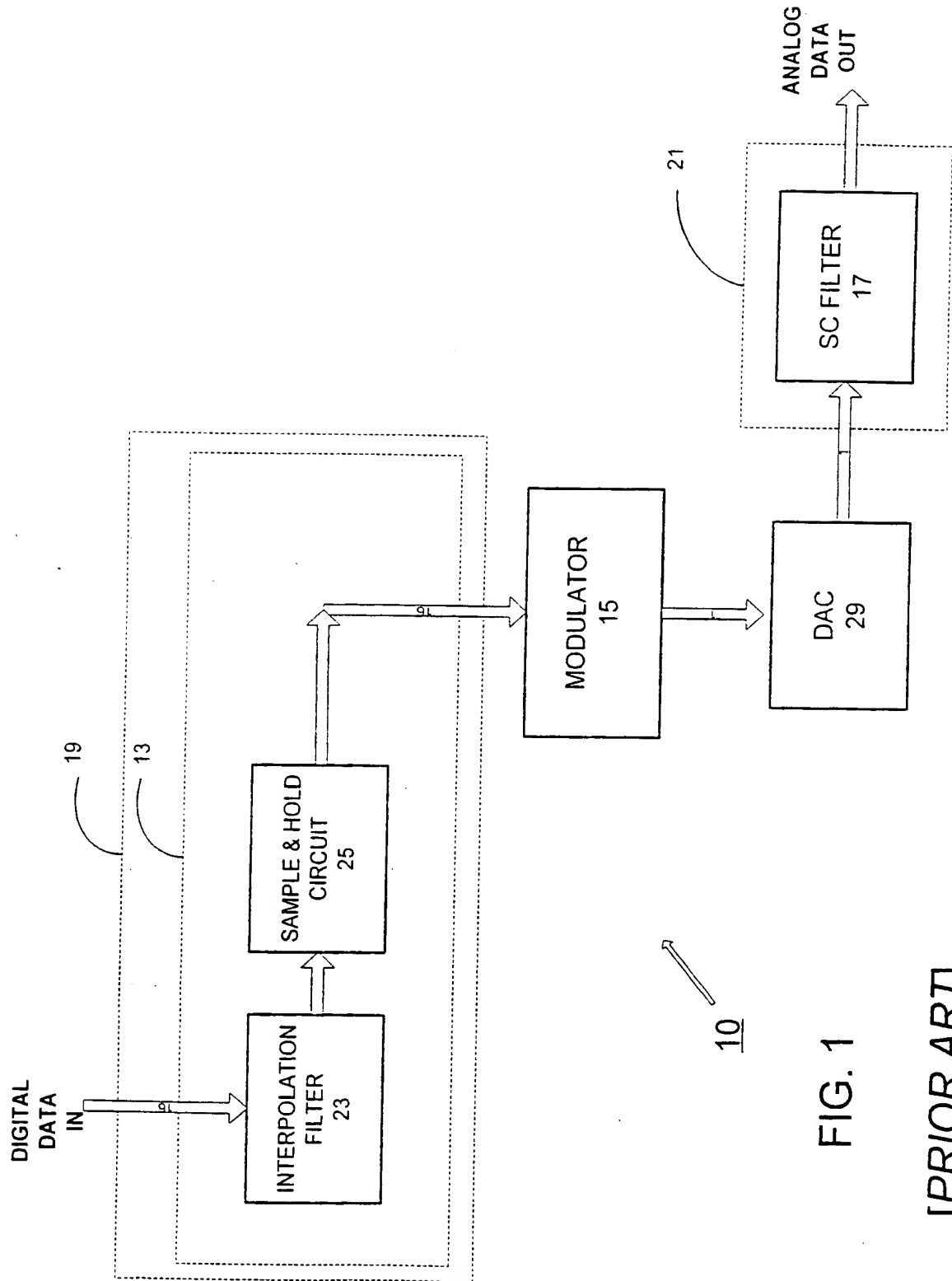
- 20 -

13.   The method of claim 12, further comprising the step
of detecting the underflow condition by testing the
status of an input data buffer.

14.   The method of claim 12, further comprising the step
of detecting the underflow condition by testing the
status of a data buffer in a portion of a downstream
circuit.

15.   An apparatus for dynamically compensating for an
underflow condition in a circuit, comprising:
       an interpolation filter to generate a number of
oversamples for an input sample;
       a master clock coupled to the interpolation
filter to control the operation of the interpolation
filter;
       a buffer to hold the input sample prior to the
generation of oversamples; and
       a monitor to test the buffer for an underflow
condition, the monitor coupled to the master clock
to stall the master clock upon the occurrence of an
underflow condition to at least partially compensate
for the underflow condition.

16.   A method of dynamically compensating for an
underflow condition in a circuit, comprising:
       sampling a signal at a sampling rate;
       oversampling the sampled signal to generate a
prespecified number of oversamples per a frame;
       changing an amount of oversampling per frame to
at least partially compensate for the underflow
condition.

- 21 -

17.   The method of claim 16, further comprising the step
       of detecting the underflow condition by testing the
       status of an input data buffer.

18.   The method of claim 16, further comprising the step
       of detecting the underflow condition by testing the
       status of a data buffer in a portion of a downstream
       circuit.

19.   The method of claim 16, further comprising the step
       of generating a number of coefficients equal to the
       prespecified number.

20.   An apparatus for dynamically compensating for an
       underflow condition in a circuit, comprising:
           an interpolation filter to generate a fixed
       number of oversamples for an input sample;
           a frame controller coupled to the interpolation
       filter to repeat at least one of the number of
       oversamples generated;
           a buffer for holding the input sample prior to
       the generation of oversamples; and
           a monitor to test the buffer, the monitor
       coupled to the frame controller to provide the frame
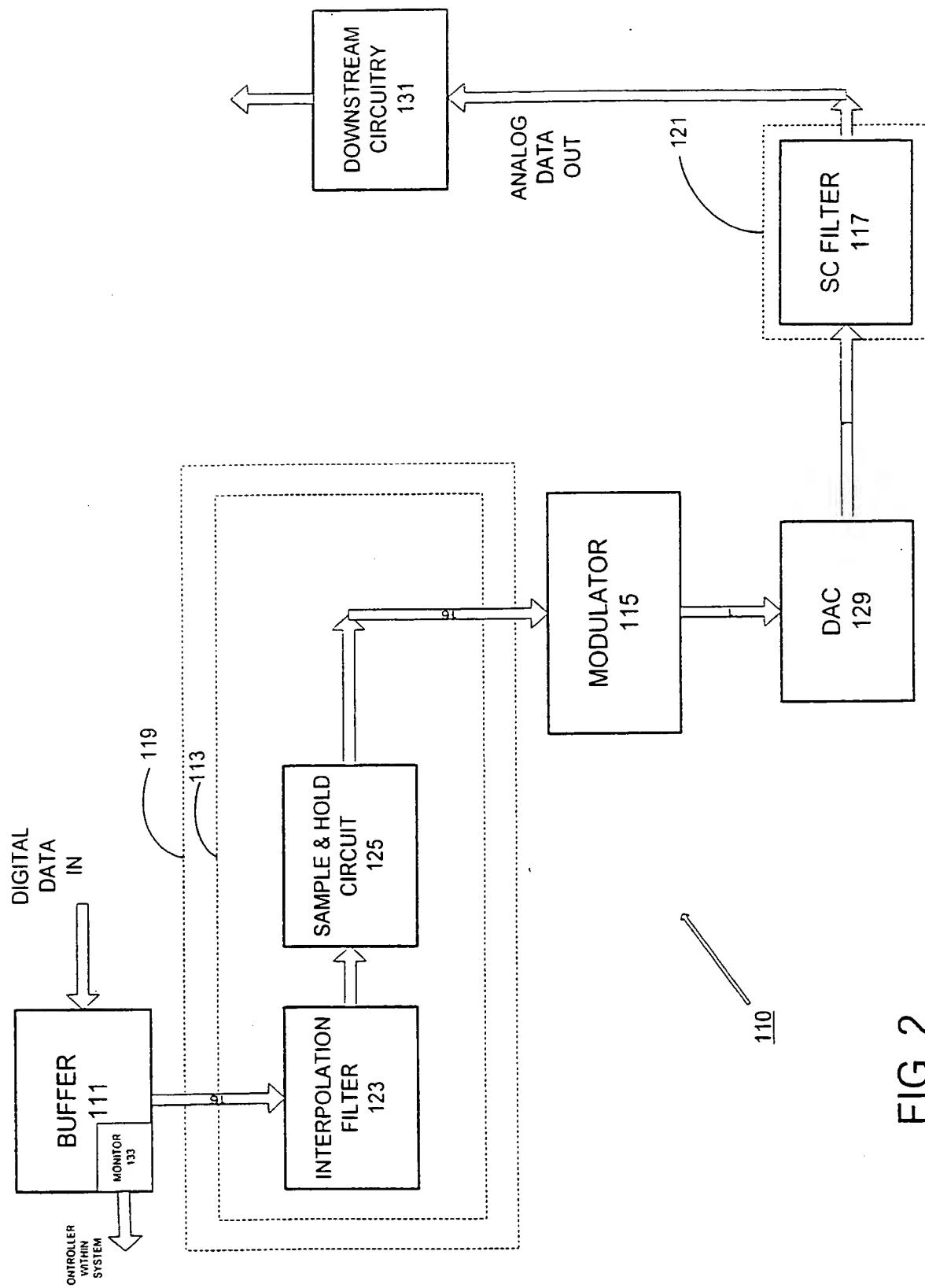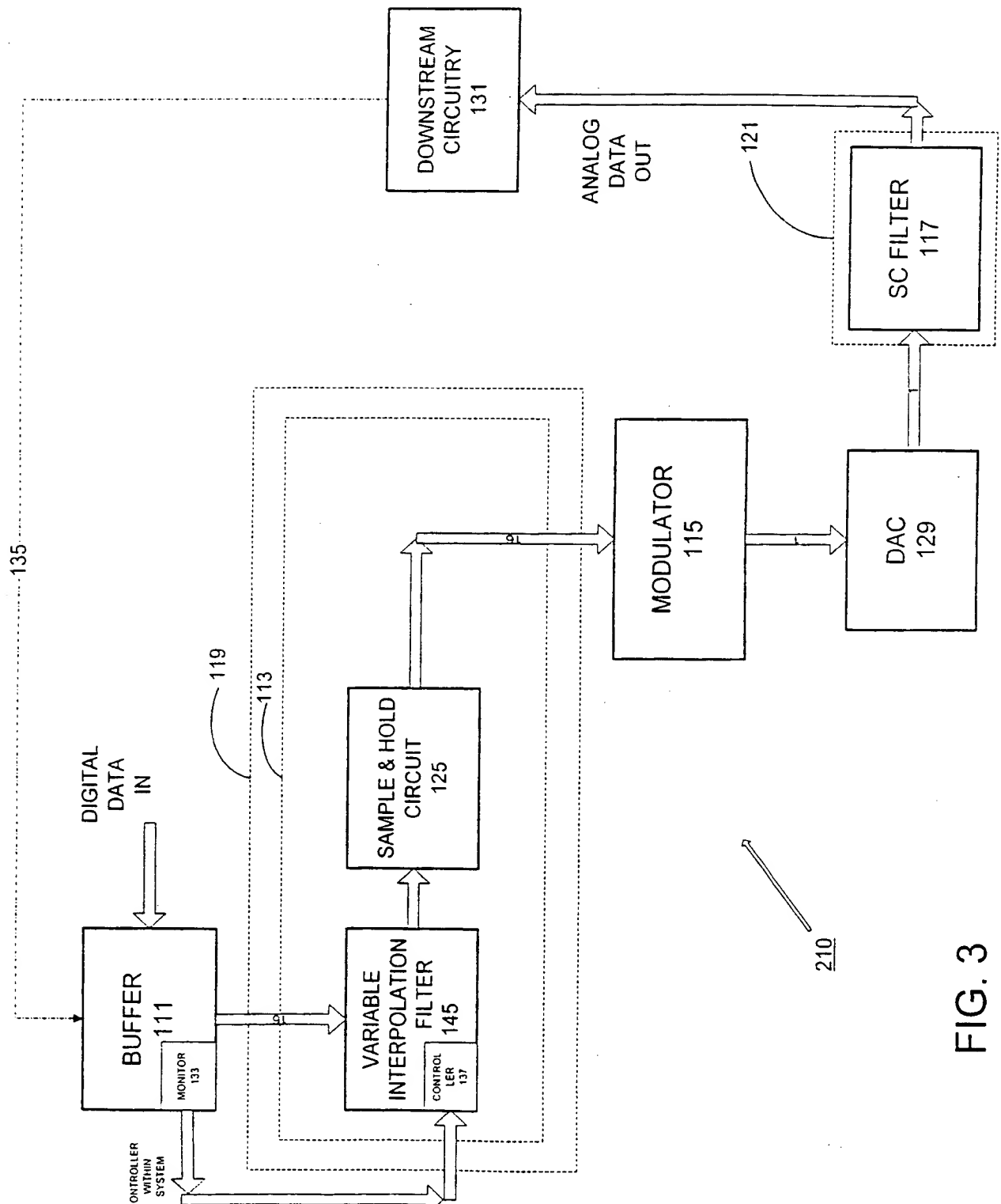   controller with an underflow condition in a circuit.
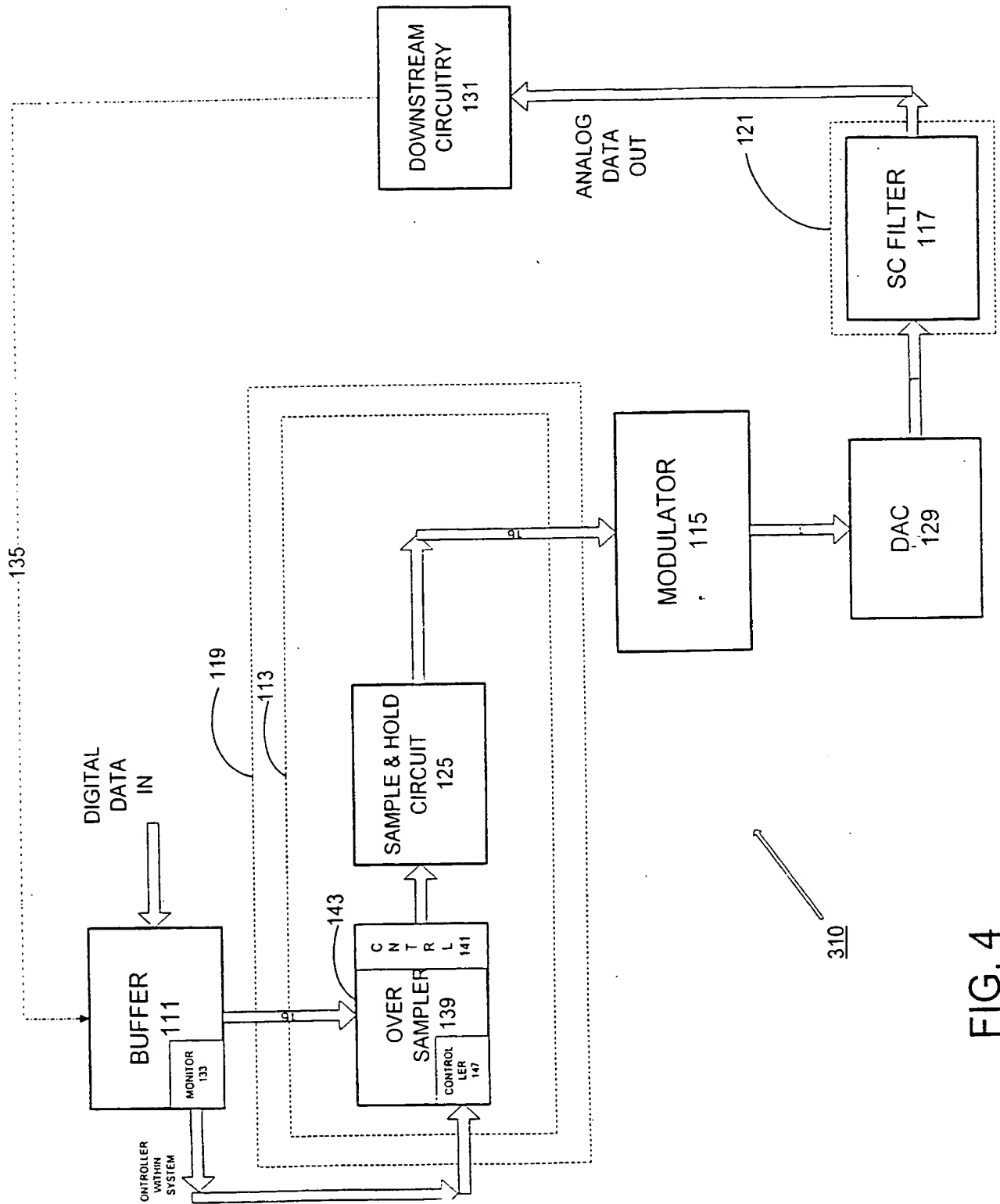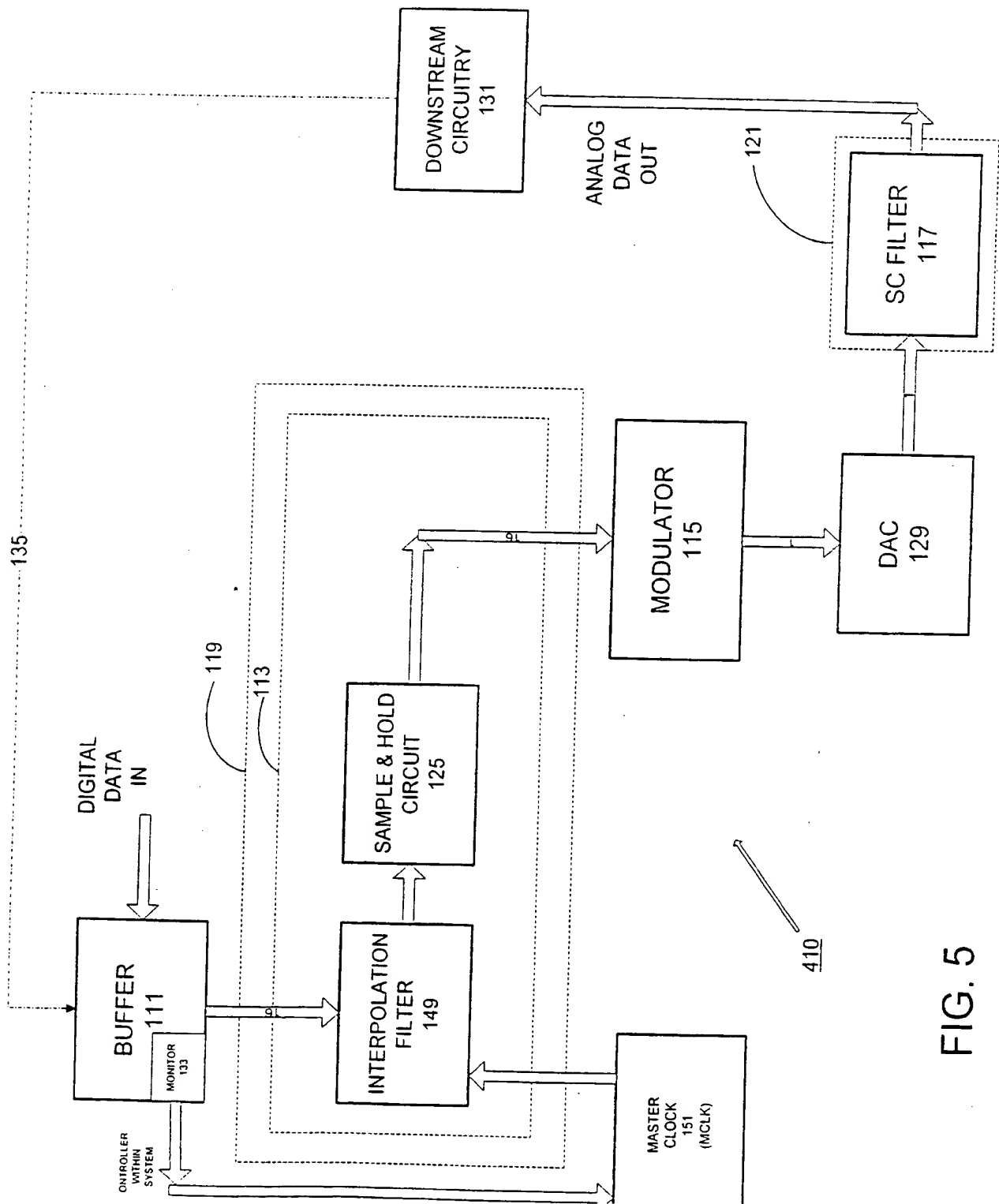
- 22 -

21.   A method of dynamically compensating for an
        underflow condition in a circuit, comprising:
                sampling a signal at a sampling rate;
                oversampling the sampled signal to generate one
   5   of a prespecified number of oversamples per a frame,
        the prespecified number equal to a nominal number in
        the absence of an underflow condition, the
        prespecified number greater than the nominal number
        in an underflow condition.

10 22.   The method of claim 21, wherein the prespecified
        number is equal to the nominal number plus one
        oversample.

    23.   The method of claim 21, further comprising the step
        of detecting the underflow condition by testing the
   15   status of an input data buffer.

    24.   The method of claim 21, further comprising the step
        of detecting the underflow condition by testing the
        status of a data buffer in a portion of a downstream
        circuit.

20 25.   The method of claim 21, further comprising the step
        of generating a number of coefficients equal to the
        prespecified number.

- 23 -

26.   An apparatus for dynamically compensating for an underflow condition in a circuit, comprising:

    a variable interpolation filter to generate oversamples for an input sample;

    a controller coupled to the variable interpolation filter to control the number of oversamples generated;

    a buffer for holding the input sample prior to the generation of oversamples; and

    a monitor to test the buffer, the monitor coupled to the controller to provide the controller with an underflow condition in a circuit.

DIGITAL
DATA
IN

INTERPOLATION
FILTER
23

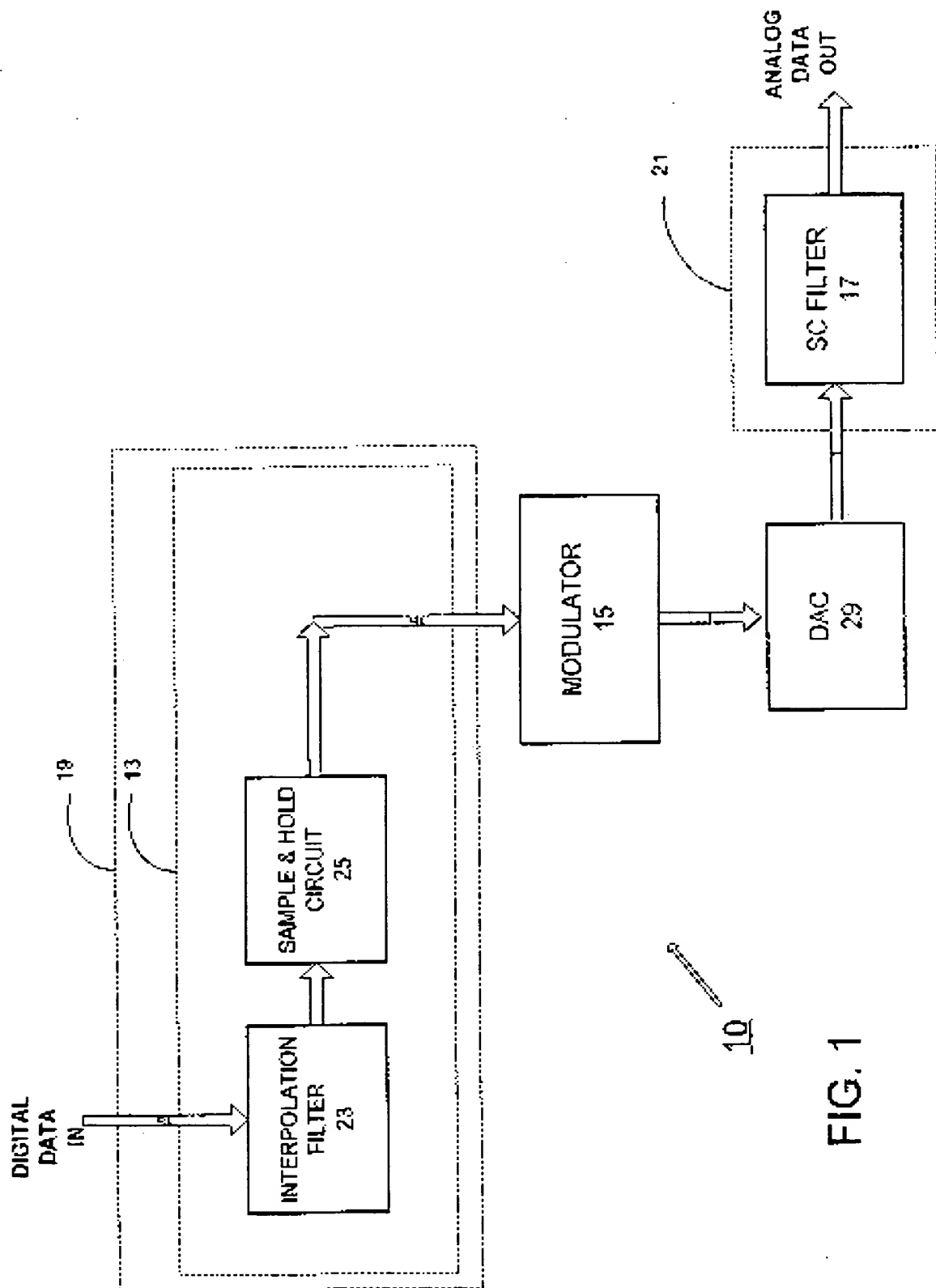SAMPLE & HOLD
CIRCUIT
25

MODULATOR
15

DAC
29

SC FILTER
17

ANALOG
DATA
OUT

19

13

21

10

FIG. 1

[PRIOR ART]

FIG. 2

FIG. 3

FIG. 4

FIG. 5

Fig. 6

Fig. 7

INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO4J 03/16, 03/22
US CL : 370/470; 360/32

According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. . 370/465,470,471,472,545 ; 360/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: sampl?, oversampl?, codec, dac, buffer or memory, frame

C.	DOCUMENTS CONSIDERED TO BE RELEVANT	

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,544,140 A (SEAGRAVE ET AL.) 06 AUGUST 1996, FIG. 2	1-26
A,E	US 5,917,917 A (JENKINS ET AL.) 29 JUNE 1999, FIG. 7	1-26
A,P	US 5,848,097 A (CARNEY ET AL.) 08 DECEMBER 1998, FIG. 3	1-26

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

.	Special categories of cited documents	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 JUNE 1999	20 AUG 1999

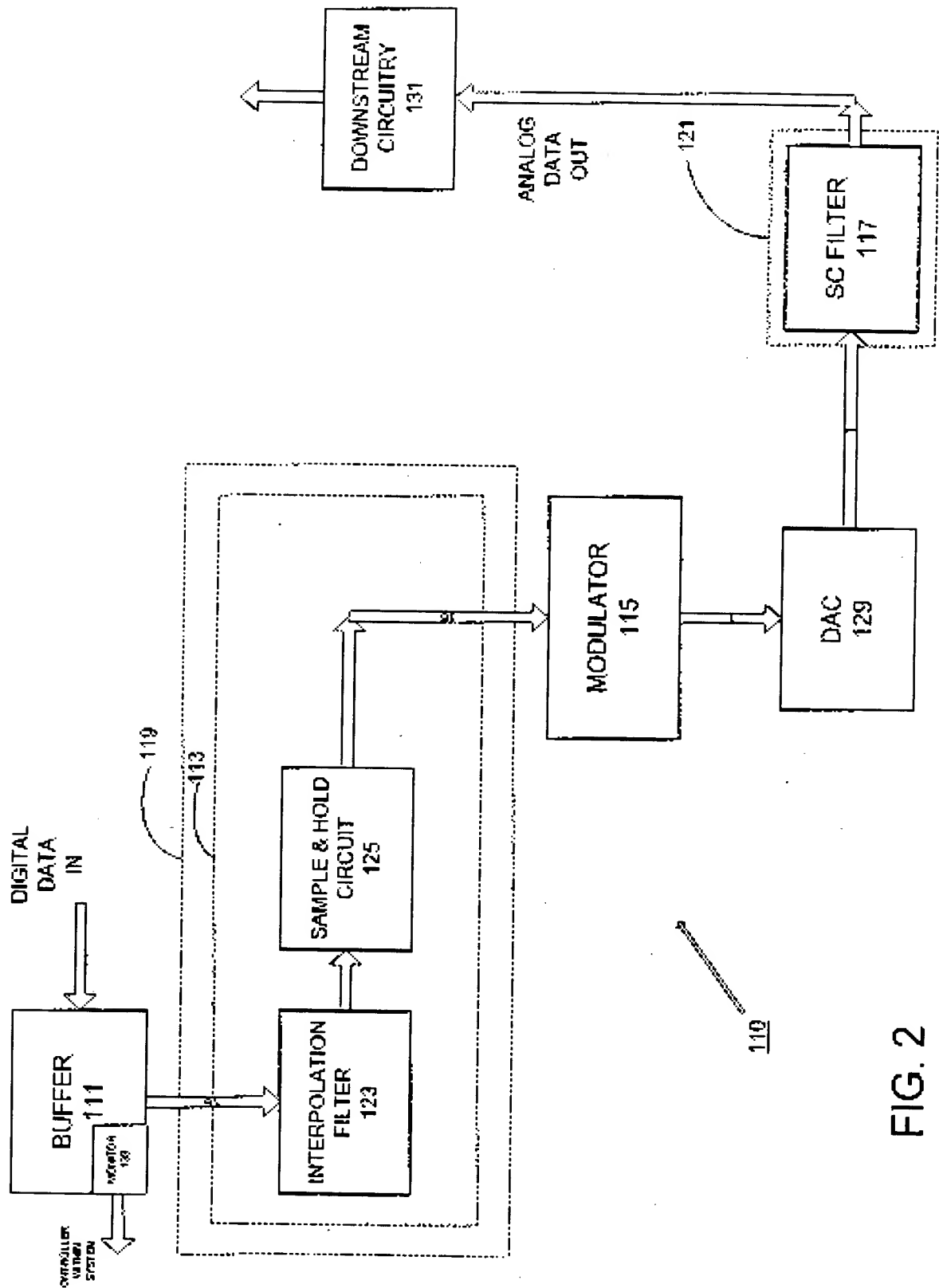| Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	SEEMA S. RA James R. Matthews
Facsimile No. (703) 305-3230	Telephone No. (703) 308-3900

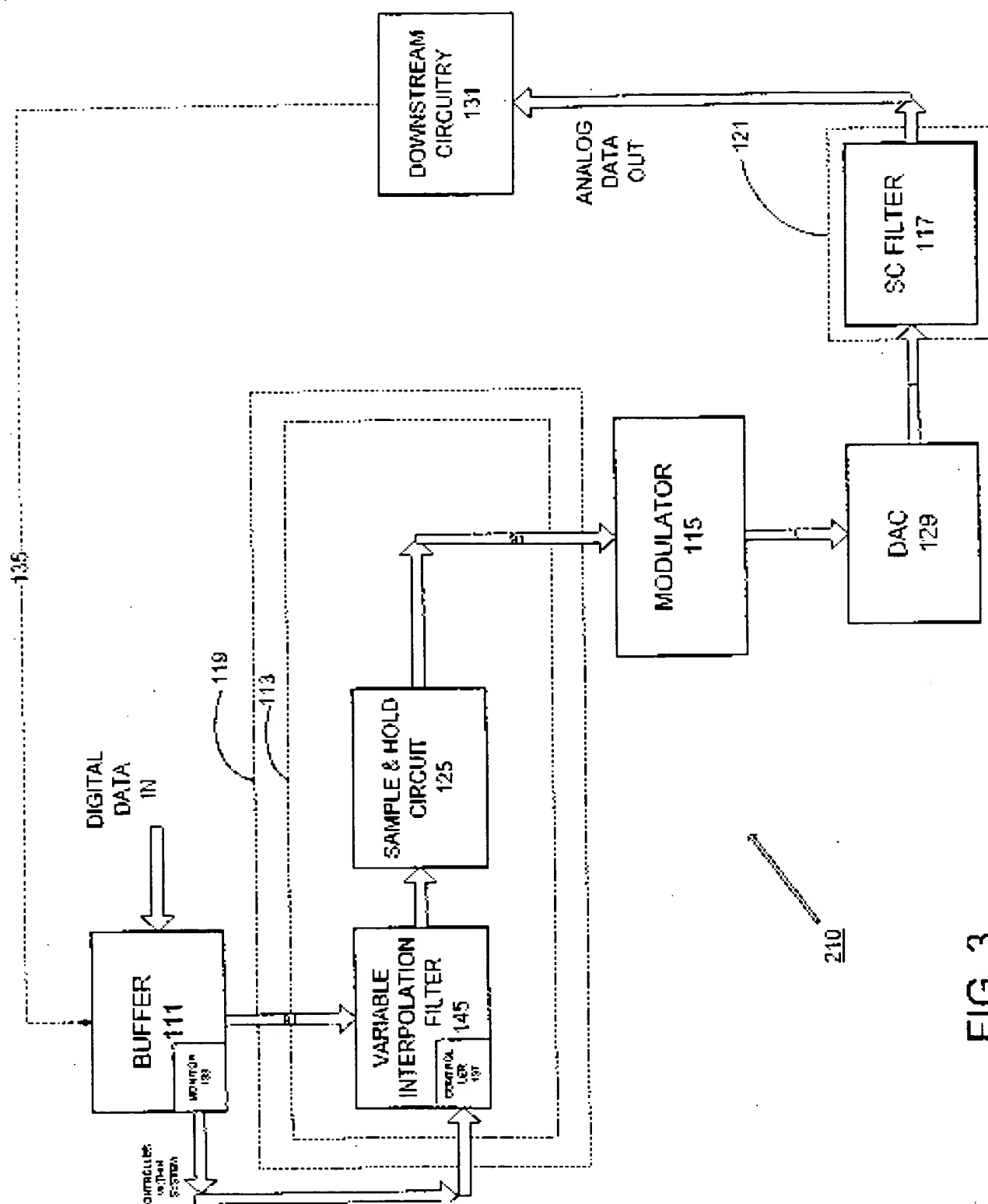Form PCT/ISA/210 (second sheet)(July 1992)*
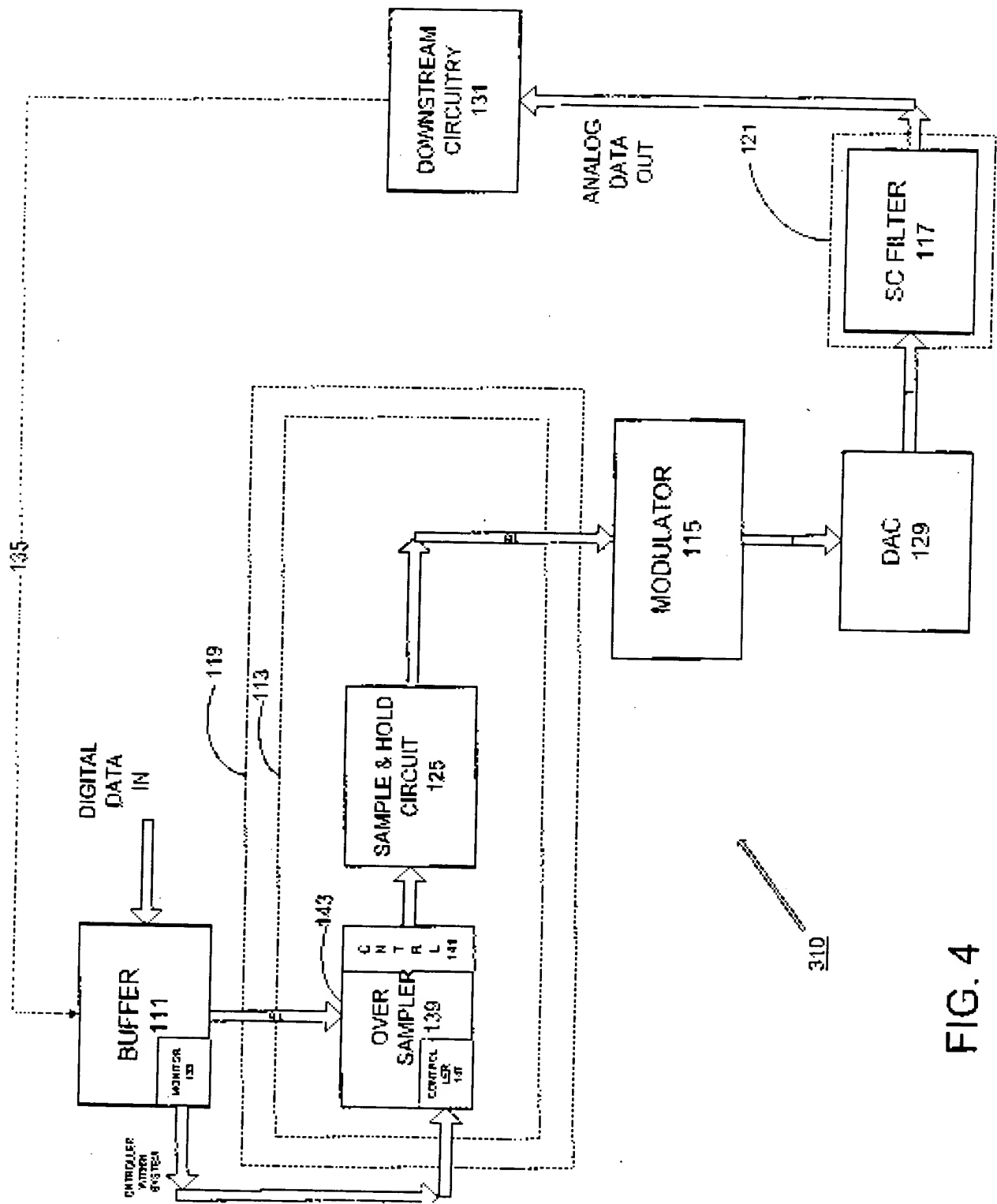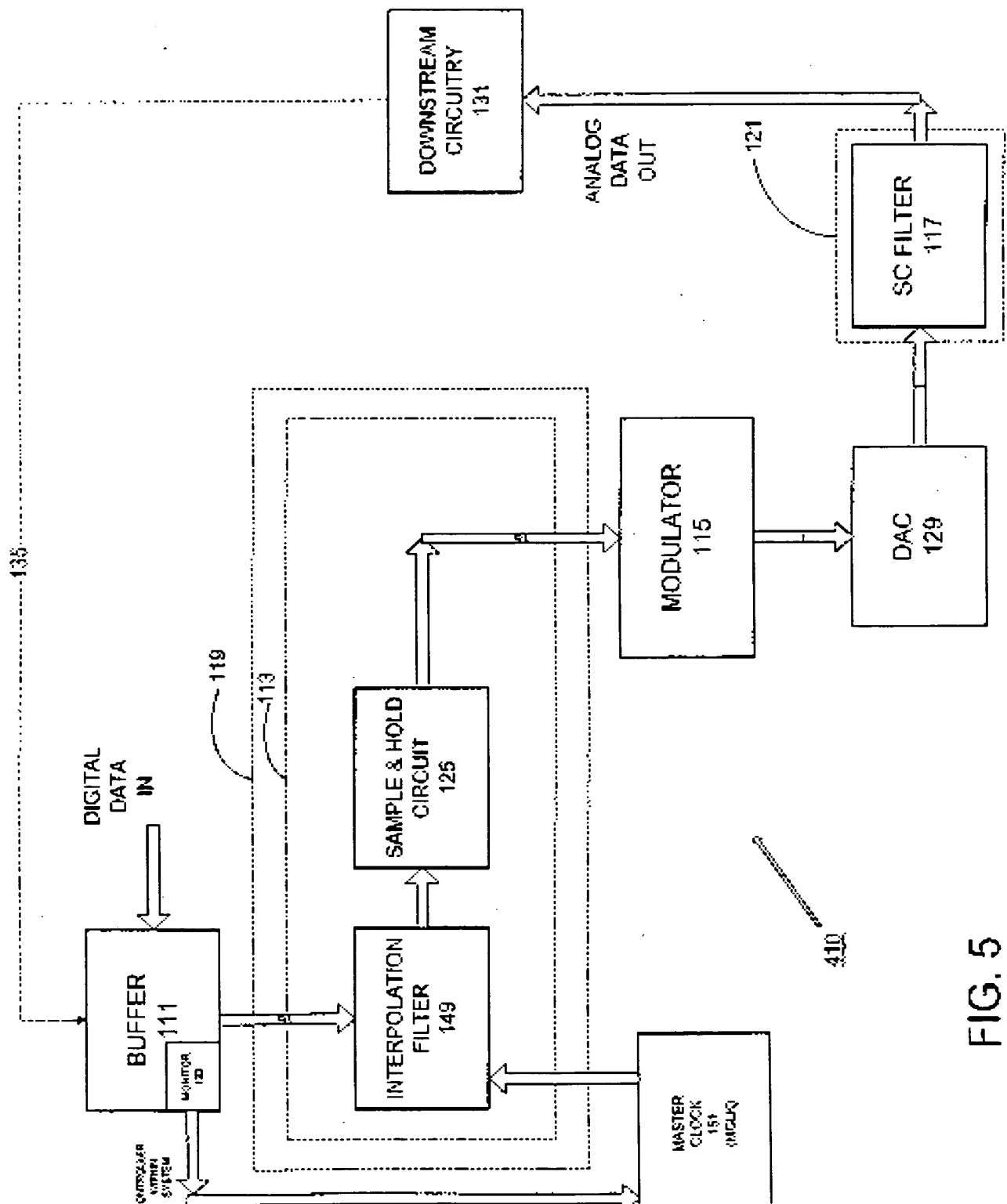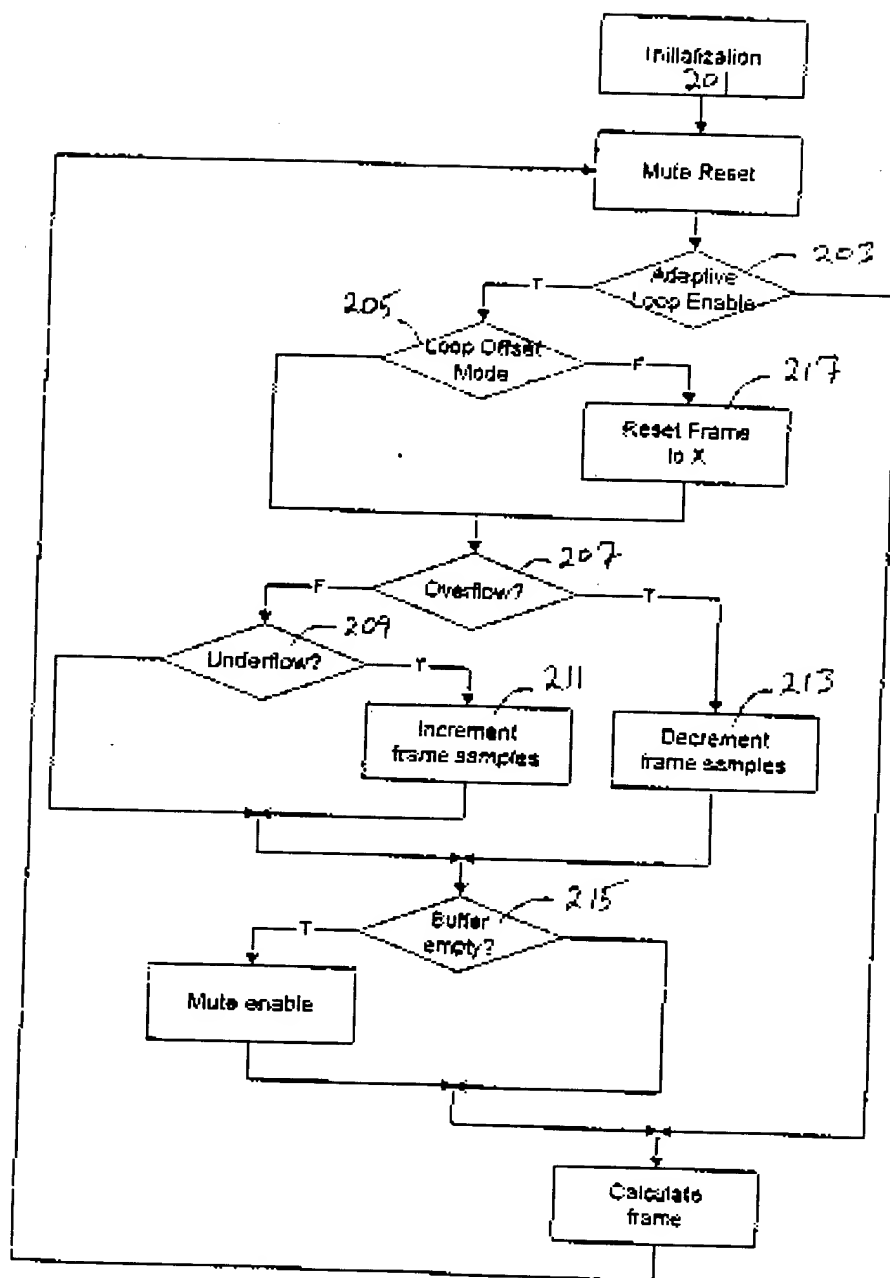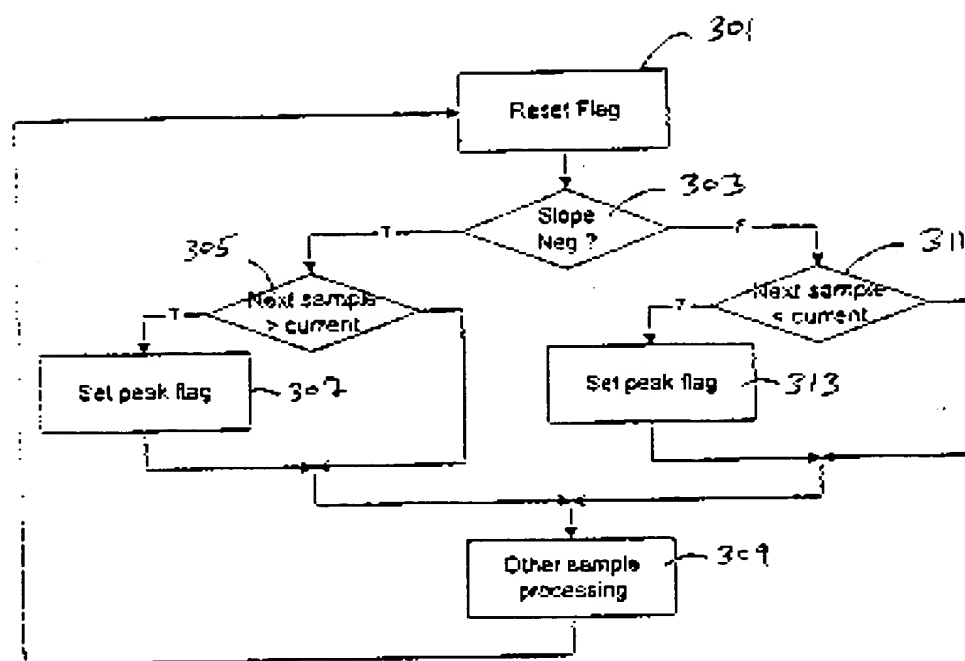
THIS PAGE BLANK (USPTO)

FIG. 1

[PRIOR ART]

FIG. 2

FIG. 3

FIG. 4

FIG. 5

Fig. 6

Fig. 7

THIS PAGE BLANK (USPTO)